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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/751,270	12/30/2003	Saikumar Jayaraman	884.888US1	7480

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EXAMINER	
TSOY, ELENA	

ART UNIT	PAPER NUMBER
1792	

MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/751,270	JAYARAMAN, SAIKUMAR	
	Examiner	Art Unit	
	Elena Tsoy	1762	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 September 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12,14-24 and 31-36* is/are pending in the application.

4a) Of the above claim(s) *21-24* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12,14-20 and 31-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on September 14, 2007 has been entered.

Response to Amendment

Amendment filed on September 14, 2007 has been entered. Claims 1-12, 14-24, and 31-36 are pending in the application. Claims 21-24 are withdrawn from consideration as directed to a non-elected invention.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Rejection of claim 9 under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention has been withdrawn due to Applicants' explanation.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 2, 4, 5, 7, 10-12, 14, 15, 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jacobson et al in view of Suda et al (US 4731855) and Kamieniecki et al (US 5661408).

Jacobson et al are applied here for the same reasons as set forth in paragraphs 8 and 14 of the Office Action mailed on 7/27/2006. Jacobson et al further teach that their method is used for the manufacture of a *semiconductor device* (See column 1, lines 14-24) by using as substrate 100 any surface sufficient smoothness that may be conveniently patterned, and which will not bond to the material from which the stamp is to be formed such as *silicon wafers*, and exposed photoresist (See column 3, lines 37-41).

Jacobson et al fail to teach *in situ* testing the substrate while attached as part of an array of substrates.

Suda et al teach that it is essential to check whether any defect is included in or any foreign material is deposited on a pattern formed on a semiconductor wafer in order to improve the yield in the manufacture of a *semiconductor device* (See column 1, lines 15-18) in the course of a production line without taking out the semiconductor device from the line; that is, they are not applicable to a process **in-line** test (See column 1, lines 50-57).

Kamieniecki et al teach that frequently, failure of an individual operation is detected only after the completion of the entire, very expensive, process of IC fabrication. Due to the very high cost of advanced IC fabrication processes, such failures result in the severe financial losses to the integrated circuit manufacturer. Therefore detection of errors in the manufacturing process, immediately after their occurrence, i.e. real-time in-line testing of semiconductor wafers during integrated circuit fabrication (See column 1, lines 5-9) allows to prevent the unnecessary continuation of the fabrication of devices which are destined to malfunction, and hence, could substantially reduce the financial losses resulting from such errors. See column 1, line 5 to column 2, line 24.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have conducted real-time in-line testing of semiconductor wafers during the manufacture of a semiconductor device in Jacobson et al without taking out the semiconductor device from the line with the expectation of reducing the financial losses resulting from errors, as taught by Suda et al and Kamieniecki et al.

5. Claims 1, 2, 4-12, 14-20, and 31-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Carter (US 6,730,617) in view of Suda et al and Kamieniecki et al.

Carter is applied here for the same reasons as set forth in paragraphs 7 and 13 of the Office Action mailed on 7/27/2006 because amended claim 35 and amended claim 36 incorporate limitations of non-amended claims 20 and 32.

Carter teaches that a polished silicon wafer can be used a substrate (See column 7, lines 55-56). Carter fails to teach in situ testing the substrate while attached as part of an array of substrates.

Suda et al and Kamieniecki et al are applied here for the same reasons as above.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have conducted real-time in-line testing of semiconductor wafers during the manufacture of a semiconductor device in Carter without taking out the semiconductor device from the line with the expectation of reducing the financial losses resulting from errors, as taught by Suda et al and Kamieniecki et al.

As to claims 20 and 35, The Examiner takes official notice that when the polymer layer is cured with a thermal radiation transmitted through the stamp, the radiation heats the subsequent polymer at a greater rate than the substrate.

As to claims 32 and 36, The Examiner takes official notice that the processed polymer layer in he cited prior art would have claimed properties, e.g. 10 % or less of a deviation from planarity, since it is prepared and processed by methods substantially identical to that of claimed invention.

It is held that where the claimed and prior art products are identical or substantially identical in structure or composition, or are produced by identical or substantially identical processes, claimed properties or functions are presumed to be inherent. See MPEP 2111.02, 2112.01. In re Best, 562 F.2d 1252, 1255, 195 USPQ 430, 433 (CCPA 1977). "When the PTOshows a sound basis for believing that the products of the applicant and the prior art are the same, the applicant has the burden of showing that they are not." In re Spada, 911 F.2d 705, 709, 15 USPQ2d 1655, 1658 (Fed. Cir. 1990).

6. Claims 3, 6, 20, 31-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jacobson et al in view of Suda et al and Kamieniecki et al, as applied above, and further in view

of Bulthaup et al (US 6,936,181) for the reasons of record set forth in paragraph 10 of the Office Action mailed on 7/27/2006.

7. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jacobson et al in view of Suda et al and Kamieniecki et al/Carter in view of Suda et al and Kamieniecki et al/, as applied above, and further in view of Walter et al (US 4,099,913) for the reasons of record set forth in paragraph 9 of the Office Action mailed on 7/27/2006.

8. Claims 6, 8, 9, 16, 20, 31-32, and 34-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jacobson et al in view of Suda et al and Kamieniecki et al, as applied above, and further in view of Carter for the reasons of record set forth in paragraph 12 of the Office Action mailed on 7/27/2006.

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Sugai (US 5440231) teaches in-line testing of non-singulated packaged semiconductor devices (See column 6, lines 14-21) although most semiconductor device manufacturers do not test the packaged semiconductor devices until after they have been singulated (See column 1, lines 24-26).

Response to Arguments

10. Applicant's arguments with respect to claims 1-12, 14-20, and 31-36 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Elena Tsoy whose telephone number is 571-272-1429. The examiner can normally be reached on Monday-Thursday, 9:00AM - 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Meeks can be reached on 571-272-1423. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Elena Tsoy, Ph.D.
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Art Unit 1762

ELENA TSOY
PRIMARY EXAMINER
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September 28, 2007